REMARKS

Claims 1-27 are pending in the present application and are rejected. In response, Claims 3, 4, 7, 11, 13, 14, 17, and 21-27 are amended, no claims are cancelled Claim 28 is added. Applicants respectfully request reconsideration of pending Claims 1-28 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

I. Objection to the Drawings

The Examiner has objected to FIGS. 1 and 19. FIG. 1 is amended to incorporate the legend – Prior Art – and FIG. 19 has been amended to correct the reference number. Replacement Sheets for FIGS. 1 and 19 are attached hereto. Therefore, Applicants respectfully request that the Examiner withdraw the objection to FIGS. 1 and 19.

Furthermore, Applicants have amended FIGS. 3, 6A and 11 to illustrate data shuffle unit 232, which was provided by Applicants' disclosure as initially filed. Specifically, as recited by original Claim 27, initial Claim 27 recites:

> a data shuffle unit to organize, in response to execution of an address shuffle instruction, address elements within the address data storage device according to a data processing operation and to organize, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation. (Emphasis added.)

Accordingly, Applicants incorporate the data shuffle unit within FIGS. 3, 6A and 11 to illustrate functionality for performing the data shuffle operations disclosed by the specification and claims. Replacement Sheets for FIGS. 3, 6A and 11 are attached hereto.

As recited by original Claim 27, the data shuffle unit was originally included in the application disclosure as initially filed. Consequently, Applicants respectfully submit that the incorporation of data shuffle unit 232 within FIGS. 3, 6A and 11 does not represent new matter. Therefore, Applicants respectfully request the Examiner allow the entry of the replacement sheets for to FIGS. 3, 6A and 11.

II. Objections to the Specification

The Examiner has objected to the specification for minor informalities. Applicants have amended the specification to correct these informalities.

The Examiner has objected to paragraphs [0031]- [0036] of the specification as being directed to a "Summary of the Invention." However, Applicants would like to kindly point out that both the M.P.E.P. and 37 C.F.R. §1.73 do not require the presence of a "Summary of the Invention" in a patent application. They merely indicate where in the application the "Summary of the Invention" should be placed if Applicants were to elect to include one. In particular, 37 C.F.R. §1.73 only states that "[a] brief summary of the invention . . . should precede the detailed description." 37 C.F.R. §1.73 does not state "must" or "shall." Accordingly, Applicants have elected not to include a "Summary of the Invention" as this is within the discretion of Applicants.

Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the objection to the specification.

III. Objections to the Claims

The Examiner has objected to the claims for minor informalities. Applicants have amended the claims to correct these informalities.

Accordingly, in view of Applicants' amendments to the claims, Applicants respectfully request that the Examiner reconsider and withdraw the objection to the claims.

IV. Claims Rejected Under 35 U.S.C. §112

The Examiner has rejected Claims 1-27 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse this rejection.

Subject matter within the specification to reasonably convey to one skilled in the relevant art, at the time the application was filed, that the inventor had possession of the claimed invention is provided with reference to at least FIGS. 2, 3, 6A-6C and 7-11. As indicated in Applicants' specification:

> FIG. 6A further illustrates the processor 209 as initially depicted in FIGS. 2 and 3 in order to illustrate the dedicated MEM device 320, as well as the register file 300. Accordingly, in the embodiment described, the computer system 200 includes a dedicated memory device 320 for storing computationally intensive operations that are calculated before application start-up or when an application is initialized. Such computationally intensive operations are utilized by encryption as well as channel code operations as described above, which may be stored in data arrays, look-up tables, storage areas or the like within the dedicated MEM device 320. (pg. 10, ¶0055, lines 1-8.) (Emphasis added.)

Applicants respectfully submit that the calculation of such computationally-intensive operations, which are used for encryption, as well as channel codes, is known in the art. However, in contrast with the conventional computation of such operations, the embodiments illustrated in FIGS. 6A-6C of Applicants' specification, store such computationally-intensive operations within data arrays, look-up tables storage areas or the like within the dedicated memory device 320.

Subsequent to the storage of computationally intensive data within MEM device 320, one skilled in the art could, based on the above passage, as well as the embodiment illustrated in FIG. 11, generate a mask, such as, for example, mask 350, as shown in FIG. 11. Using such a mask, data shuffle unit 232 may perform a data shuffle operation to arrange addresses, such as, for example, address indices. As shown in register 310-1 of FIG. 7, address indices could be organized to populate an address register, such as R_0, address register 310, as shown in FIGS. 6A-6C. As further described in Applicants' specification:

> The multiple-data operation set enables loading of data within destination register R_1 310-2, that is randomly distributed within storage areas 330 (330-1, . . ., 330-N) of the dedicated memory device 320. Accordingly, once computationally intensive operations are stored within storage areas 330, an application utilizing or requiring the computational results will load the desired results within a destination register 310 based on, for example, address indexes which are stored in address register (R_0) 310-1. As such, the execution unit 230 will receive an address index, as well as other information, in order to access data elements within the storage areas 330 and store those requested data elements within the destination register 310. (pg. 10, ¶0056, lines 3-12.) (Emphasis added.)

As indicated by the above-cited passage, the execution unit will receive an address index to access data elements within the storage areas 330 and store the requested data elements within destination register 310. The execution unit 230, as shown in FIG. 6A, in response to receiving, for example, a move multiple instruction, populates destination register 310-2 according to address indices within address register 310-1. The indexing of storage areas 330-1 to 330-N, as shown in FIG. 6A, is performed according to the address indices, offsets and tableN operands, as shown in FIG. 6B of Applicants' specification. As further described by Applicants' specification:

> In one embodiment, a multiple move operation: MOV MULTIPLE R_0, [R_1, offset, tableN] directs the loading of multiple, randomly distributed data within the dedicated memory device 320 as depicted in FIGS. 6B and 6C. Accordingly, the R_0 argument indicates the address register 310-1 which contains

address indexes for capturing data within the storage areas 330, which in one embodiment are configured as look-up tables. The R_1 argument indicates the destination register 310-2 wherein to store the data elements which are read from the storage areas 330 of the memory device 320. The offset argument indicates an area 334 (334-1, . . ., 334-N) within which the look-up table 330 has been divided. Finally, the tableN argument 336 indicates the table 330 within the memory device 320 which contains the data. For example, FIG. 6C depicts a 1024 byte table 330 with a 256-byte address index 332 and a two bit offset 334. (pg. 10, ¶0057, lines 1-11.) (Emphasis added.)

Accordingly, based on the cited passage above, as shown in FIG. 6A, execution unit 230, in response to MOV_MULTIPLE instruction, loads data from storage areas 330 according to address register 310-1 within destination register 310-2. Representatively, MOV_MULTIPLE instruction includes the R_0 address register 310 argument, the destination register argument R_1 and offset, which includes an area 334 within each look-up table 330, for example, as shown in FIG. 6B, and finally the tableN argument 336, which indicates the table within the memory device, which contains the data.

In addition, Applicants have amended FIGS. 3, 6A and 11 and provide replacement sheets for FIGS. 3, 6A and 11, to illustrate data shuffle unit 232. Applicants respectfully submit that the incorporation of the data shuffle unit into FIGS. 3, 6Aand 11 does not represent new matter since data shuffle unit 232 was included within the application as initially filed. Specifically, as recited by Claim 27 prior to amendment, Claim 27 recites:

> a data shuffle unit to organize, in response to execution of an address shuffle instruction, address elements within the address data storage device according to a data processing operation and to organize, in response to executing a data shuffle instruction, data elements within the destination data storage device according to a data processing operation.

Accordingly, since a data shuffle unit was originally included in the application disclosure as initially filed, Applicants respectfully submit that the incorporation of a data shuffle unit within FIGS. 3, 6A and 11 does not represent new matter. Therefore, Applicants respectfully request the Examiner allow the entry of the data shuffle unit to replacement sheets for FIGS. 3, 6A and 11 attached hereto.

Applicants respectfully submit that one skilled in the art, based on the above-cited passages of Applicants' specification and at least FIGS. 3 and 6A-11, would be reasonably conveyed information for loading randomly stored data from storage areas 330 to a destination register according to an address register. Hence, Applicants respectfully submit that the claims contain subject matter, which was described in the specification in such a way as to reasonably

convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention.

Consequently, Applicants respectfully submit that Claims 1-27, as filed, comply with the written description requirement. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph, rejection of Claims 1-27.

The Examiner has rejected Claims 1-27 under 35 U.S.C. §112, first paragraph, as failing to comply with the enabling requirement. Applicants respectfully traverse this rejection.

For at least the reasons provided above, Applicants respectfully submit that at least ¶¶0055-0057, as well as ¶¶0084-0085 of Applicants' specification clearly convey the capability to load a register with address indices, which along with a destination register operand, offset operand and a tableN operand can be used to direct an execution unit to load randomly stored data from a dedicated memory device to a destination data storage device.

Consequently, Applicants respectfully submit that Claims 1-27, as filed, contain subject matter that was described in the specification in such a way so as to enable one skilled in the art to which it pertains or with which it is more nearly connected, to make and/or use the invention. The single multiple data load instruction, assuming it is provided with the proper operands, for example, as described in at least ¶¶0055-0057, as well as ¶¶0084-0085, may use the various operands of the move multiple instruction, as described in ¶¶057 to take multiple random located data from a memory device and load the data within a destination data storage device in response to a multiple data load instruction.

Accordingly, Applicants respectfully submit that Claims 1-27, as filed, comply with the 35 U.S.C. §112, first paragraph enablement requirement. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the 35 U.S.C. §112, first paragraph, rejection of Claims 1-27.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-28 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: February 10, 2006

By: _____
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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 10, 2006

Marilyn Bass February 10, 2006